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Serial Command Link Distribution Card for the ADF system

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1/ Introduction

The Serial Command Link Distribution Card (SCLD) is a board to be used in the upgrade of the D0 L1 Calorimeter Trigger at Run IIb. It provides the interface between the central distribution network for clock and timing signals in D0 called the "Serial Command Link" (SCL) [1], and the ADF system [2]. The main functions of the SCLD are the following:

- (a). Receive from the SCL and distribute to the ADF system the D0 beam-crossing clock with a phase that ensures the correct synchronization of the whole ADF system;
- (b). Receive from the SCL and distribute to the ADF system various signals: geographic section initialization, L1 accepts, beam crossing counter marker...
- (c). Receive from the ADF system status and error signals, combine these and send them over the SCL to the D0 Trigger Control Computer;
- (d). Receive from one ADF board (or a subset of ADF boards) intra-ADF control signals, combine and distribute them in a synchronous way to all ADF boards.

The SCLD board is made in 6U VME mechanical format. It uses only the +5V supply from the backplane and does not interact with VME signals. The board does not need to be configured or monitored at run time. FPGA firmware is loaded upon power-up. The few adjustable parameters of the board are stored in a flash memory that can be reprogrammed via JTAG.

2/ Functions of the card

2.1/ Global ADF system synchronization

The whole ADF system is synchronized with the D0 experiment by the 7.57 MHz beam crossing clock. The ADF system has to guarantee that the digital values output every BC period for the 2560 calorimeter channels correspond exactly to the same beam crossing period. To achieve this, propagation delays for all analog signals and ADC sampling clocks must be equalized. The cables carrying the analog signals cannot be perfectly matched. The spread in time for the "earliest" tower compared to the "latest" one is ~80 ns. For the distribution of the clock signal, no delay compensation is made between ADFs card or within the different channels on each ADF card. The delay path skew from the SCLD to the clock input of any ADC on any ADF board is expected to be ~2 ns (time propagation on 1:2 length of the VME backplane + skew for the channels on the same ADF board). The maximum static spread in time between any two channels is expected to be less than ~82 ns. Some additional jitter (especially on the analog signals) will increase the spread, but it is anticipated that the peak-to-peak value will be less than a BC period (132 ns). This is mandatory to guarantee that the assignment of energy values computed by the ADF to each beam crossing can be made in a non-ambiguous way. For the ADF system, a beam-crossing starts on the rising edge of the BC clock and ends on the next rising edge. In that interval of time, it is expected that all channels for that beam crossing have been sampled. The signal of the "earliest" tower and that of the "latest" tower for the current beam crossing must be located in the same 132 ns time window. The adjustment is made by a static delay applied to the BC clock received over the SCL before distributing it to the ADF system. The phase shift range shall be 0 to 132 ns, in steps of ~4ns or less.

2.2/ SCL signal distribution

Asynchronous signals can be sent to the ADF system over VME. Synchronous (to the BC clock) signals are delivered by the SCL. The synchronous SCL signals of interest for the ADF system are the following:

- the 7.57 MHz BC clock with a calibrated phase (see above)
- L1 trigger accepts. These are used by the ADF to initiate the transmission of

raw ADC data to the TAB, or to freeze the content of history buffers in the ADF to monitor the operation of digital filters.

- one or several L1 qualifier bits. These are used to distinguish between L1 accepts that do not cause history buffers to freeze and L1 accepts for monitoring that will cause recording in history buffers to stop. It has not yet been decided yet which of the qualifier bit among the 16 delivered by the SCL will be used.

- The first period marker. This marker indicates that the current beam crossing is the first one in the current turn (159 crossings per turn). The ADF system keeps track of beam crossing numbers. The local value in each ADF board is sent for each beam crossing to the TAB. Checking that all the received beam crossing counts are equal allows to detect synchronization errors.

The asynchronous SCL signal "initialization request" is also delivered to the ADF system. Both the SCLD and the ADF system shall perform some initialization and return an initialization acknowledge to the SCL.

2.3/ ADF control/error signal concentration and forwarding to the SCL

Each ADF card can assert a busy signal (SCLIF_BUSY_B_OUT), an error signal (SCLIF_ERR_B_OUT) and an init acknowledge signal. Busy and error signals are OR-wired at the level of each ADF crate. These signals are then OR-ed by the SCLD and sent back to the SCL. Init acknowledge signals are AND-ed before being forwarded to the SCL. The SCLD shall be able to drive any of the status line of the SCL. Although a number of SCL signals are not used by the ADF system at present, some of them should be connected to the SCLD for later improvements.

2.4/ Intra-ADF signals combination and synchronous fanout

Several signals can be produced by one or several ADF boards and have to be distributed in a synchronous way to all ADF boards. The SCLD is used for that purpose. Each ADF card can assert a self trigger signal (SCLIF_STRIG_B) whenever the ADC input of any channel exceeds a programmable threshold. This signal is OR-wired at the level of each ADF board and crate and sent to the SCLD. The SCLD makes the OR of these signals and sends the output to all ADF boards synchronously. The self trigger signal can be used to freeze the content of history buffers in the ADF to take a full snapshot of the current state of the system. Any of the ADF cards attached to the SCLD can also generate a "software L1 trigger" upon write over VME to a particular register. Software generated L1 triggers are received by the SCLD and bounced-back to all ADF cards synchronously. These L1 triggers are equivalent to D0 level 1 trigger accepts. They are used to test the ADF system independently of the D0 Framework. When history buffers in each ADF board have been frozen (e.g. following a L1 accept with monitoring request) they can be read-out over VME. To resume recording, a synchronous command has to be issued to the ADF system. This is accomplished in the same way as distributing L1 software triggers.

3/ Design and implementation constraints for the SCLD

The SCLD is a 6U card that plugs in a standard VME crate. The board does not have a VME interface and shall use only the +5V power supply. The SCLD receives a SCL Receiver mezzanine card and can be attached to up to 5 ADF crates using 8-pair differential cables with 2 mm hard metric connectors (similar to the cables used to link the ADFs to the TABs). LVDS signalling is used. The SCLD has one port that emulates the connection to an ADF crate. This is used to test the SCLD in standalone mode with a loop-back cable. The preferred connectors on the front panel to connect cables are 55-pin right angled male 2 mm hard metric types (AMP 106012-1 or equivalent). Each connector accommodates 2 connections to ADF crates. There shall be 3 connectors of this type on the front panel: 5 ports for cables to ADF crates + 1 port for loop-back test. An LED is placed next to each port to indicate cable detection. An additional visual indicator may be placed. Other elements on the front panel include at least a power-supply indicator, a RESET and an INIT push button, a JTAG connector (the pinout should allow a Xilinx Cable IV to be directly attached). All the logic of the SCLD is implemented in a single Xilinx Virtex II FPGA. The recommended target is XC2V500 FG456-4C although a smaller device would be sufficient. This choice is made to reduce the diversity of components used in the ADF system. The firmware shall be downloadable over JTAG during development and stored in a flash serial PROM for production. That PROM should be re-programmable over JTAG. Programmable

parameters are also to be stored in an external serial PROM. Model XC18V04 for both PROMs is recommended. Because Virtex II devices do not have 5V compatible I/O pins, translation to 3V3 to interface to the SCL Receiver mezzanine card is suggested. A PLL for BC clock multiplication should be included on the SCLD board (possibly to generate a BCx4, or BCx8 or BCx16 clock). The SCLD shall also include a 100 MHz local oscillator (to provide a reference clock or to allow operation without the SCL Receiver mezzanine card). Virtex II devices need 3.3 V and 1.5 V power supplies. These shall be derived from the 5V available on the VME backplane using (preferably) low dropout voltage regulators. A logic analyzer or external circuitry can be connected to the SCLD on a debug I/O port (3V3 low voltage CMOS standard).

3/ Reduced version of the SCLD

Due to development schedule constraints, a reduced version of the SCLD has been developed prior to the design of the full 6U card. The reduced version has the full functionality of the final SCLD but can be connected only to 1 ADF crate. The reduced SCLD is a mezzanine card that accepts an SCL Receiver mezzanine card on the top and that plugs on a Virtex II evaluation kit from Memec [4]. The evaluation kit includes a 1M gate Virtex II device, a JTAG configuration PROM, power supplies and de-coupling, push buttons and LEDs... The reduced version of the SCLD is therefore very simple and could be developed very quickly: it includes only 5V to 3V3 buffers for SCL signals, a JTAG PROM to store application specific parameters, a PLL for clock multiplication and various connectors. Schematics and photos of the card can be found in [3].

6/ SCLD to ADF link

Communication between the ADF system and the SCLD card is done over 8-pair 2mm hard metric cables using LVDS. Information is flowing both downstream from the SCLD to the ADF and upstream from the ADF to the SCLD. Because the number of signals to transport for each beam crossing exceeds the number of wires available, 2 pairs of wires carry frames of 8 bits. The pair carrying the BC clock operates at 7.57 MHz, while the 2 pairs carrying the time multiplexed commands operate each at ~60 Mbps. This is far below the capability of LVDS I/O's on Virtex II devices and direct end-to-end FPGA pin connection is used. . To detect cable insertion at both ends, a pair is split in two independent wires. On the SCLD side, the SCLD senses SCLD_CABLE_REM_B to detect the presense of the remote ADF card (low means board present). The SCLD has SCLD_CABLE_LOC_B hardwired to a low level to signal its presense. On the ADF side, the role of the 2 pins is symmetric. The ADF senses SCLIF_CABLE_REM_B to detect a remote SCLD card and it asserts low SCLIF_CABLE_LOC_B to signal its presense (this signal is not hardwired but driven by the logic). Cable pair usage is the following:

SCLD side Signal	Direction	ADF side Signal	Usage
SCLD_CABLE_LOC_B	SCLD->ADF	SCLIF_CABLE_REM_B	Cable detection on ADF side
SCLD_CABLE_REM_B	ADF->SCLD	SCLIF_CABLE_LOC_B	Cable detection on SCLD side
SCLF_CLK7_P	SCLD->ADF	SCLIF_CLK7_P	Master BC clock for the ADFs
SCLF_CLK7_N	SCLD->ADF	SCLIF_CLK7_N	
SCLF_CMDD_OUT_P	SCLD->ADF	SCLIF_CMDD_IN_P	Commands from SCLD to ADFs
SCLF_CMDD_OUT_N	SCLD->ADF	SCLIF_CMDD_IN_N	
SCLF_CMDU_IN_P	ADF->SCLD	SCLIF_CMDU_OUT_P	Commands/status from ADFs to SCLD
SCLF_CMDU_IN_N	ADF->SCLD	SCLIF_CMDU_OUT_N	
SCLF_BUSY_B_IN_P	ADF->SCLD	SCLIF_BUSY_B_OUT_P	Status line from ADF's
SCLF_BUSY_B_IN_N	ADF->SCLD	SCLIF_BUSY_B_OUT_N	
SCLF_STRIG_B_P	ADF->SCLD	SCLIF_STRIG_B_P	Self-trigger line from ADF;
SCLF_STRIG_B_N	ADF->SCLD	SCLIF_STRIG_B_N	
SCLF_ERR_B_IN_P*	ADF->SCLD	SCLIF_ERR_B_OUT_P*	Status line for ADFs to signal errors
SCLF_ERR_B_IN_N*	ADF->SCLD	SCLIF_ERR_B_OUT_N*	
SCLF_SPARE_OUT_P*	SCLD->ADF	SCLIF_SPARE_IN_P*	Spare line

SCLF_SPARE_OUT_N* SCLD->ADF SCLIF_SPARE_IN_N*

*: because of limitations on the number of LVDS I/Os on the Virtex-II evaluation kit, these pins are not connected on the reduced version of the SCLD. Note also that the SCLIF prefixed signals and the SCLD prefixed signals have erroneously been swapped on the connector of the reduced SCLD. This has no effect because these pins are unconnected, but must be corrected for the full version of the SCLD card.

Refer to the information available in [3] for the exact pair numbering and labelling scheme. Double check the pinout using the schematics of the ADF as a reference.

7/ Command format and serial communication

For each BC period, the SCLD sends an 8-bit command "downstream" to the ADF system using the CMDD lines. Similarly the ADF sends an 8-bit command "upstream" to the SCLD on CMDU lines. Bit usage is given below.

Command Downstream (SCLF -> ADF)

bit 0: Init Request (D0 framework Geographical Section Init)
bit 1: Resume Recording, made by 1 ADF to be fanout to all ADF's
bit 2: L1 accept generated by software, made by 1 ADF, to be fanout to all ADFs
bit 3: L1 self trigger, made by any ADF, to be fanout to all ADF's
bit 4: L1 accept with monitoring, made by D0 framework
bit 5: L1 accept (monitoring not requested), made by D0 framework
bit 6: BX marker, made by D0 framework, indicates first BC in a turn
bit 7: spare

Command Upstream (ADF -> SCLF)

bit 0: Init Acknowledge - returned by the ADF following Init Request
bit 1: Resume Recording - resume recording of data in history buffers
bit 2: Software L1 trigger - L1 accept generated by the ADF control software
bit 3: unused
bit 4: unused
bit 5: unused
bit 6: unused
bit 7: unused

At the receiver side, the LSB of each command is assumed to be present on the rising edge of the BC clock. The next bit is placed 1:8th of a BC period later. De-serialization is a bit complex and is different on the ADF and SCLD side. On the ADF side, the command sent downstream is received by FPGA#0 on the ADF board connected to the SCLD. Similarly the master BC clock is received by the same FPGA. However, the BC clock must be distributed to all ADF boards within the crate before it is used by the logic of the ADF. The fanout to the VME backplane, distribution to each FPGA and clock multiplication by 8 introduces a delay with respect to the streams received over LVDS. Because the multiplied version of the delayed BC clock is used to de-serialize the command coming from the SCLD, this bit stream should be delayed to compensate for the shift. It is expected that this delay is made by the SCLD; i.e. the SCLD will shift the LSB of the current command some amount of time after the rising of the BC clock so that the recovered BC clock is phase aligned with the LSB of the command at the ADF side. De-serializing the command sent upstream by the ADF requires the SCLD to perform the same type of phase alignment. The SCLD uses its own local BC clock to de-serialize CMDU. The phase shift depends on the propagation time through the cable that links the SCLD to the ADF as well as the delay introduced by the clock fanout circuitry within the ADF crate.

So not only the phase of the BC clock supplied to the ADF with respect to the BC clock supplied by the SCL Receiver mezzanine needs to be adjusted, but also the relative phase between the BC clock supplied to the ADF and the bit streams going upstream and downstream. Note that tuning the delay parameters must be not be inter-dependant operations: when proper de-serialization is achieved at both

ends, the phase of the BC clock at the level of the ADF w.r.t to the BC clock given by the SCLD shall be adjusted without affecting the operation of the serial communications between the SCLD and the ADF system. Assuming that the SCLD can operate with a BC clock of up to 7.8125 MHz (i.e. 128 ns period), the duration of each bit on the serial link is 16 ns. Phase adjustment by steps of 4 ns seems adequate.

8/ SCLD logic and clocking scheme

The operations performed by the SCLD are rather simple but require to introduce calibrated delays. Instead of using programmable external delay lines, the idea is to run the SCLD FPGA logic at a fast rate, and emulate delay lines in logic. Running at BC x 16 and having the possibility to clock data on the rising or falling edge of the clock leads to phase adjustment in 4 ns increments. The SCLD generates internally a BC clock x 16 (121.12 MHz nominal, 100 MHz in standalone debug mode) using a Digital Clock Manager (DCM) in the FPGA. On the reduced version of the SCLD, this clock is generated from a BC x 4 input clock (30.28 MHz nominal, 25 MHz in standalone debug) made by an external zero-delay PLL (CY 2308-3) from the 7.57 MHz (6.25 MHz in debug mode) BC clock. A second DCM is also used internally to make a shifted version of the BC x 16 clock. Phase shift is programmable in steps of 1:256th of period (i.e. ~30 ps). This feature for fine tuning of the phase may or may not be used. Although the operation of DCMs is rather stable with the reduced version of the SCLD, it would be preferable on the full SCLD to have the possibility to generate the BC x 16 clock with an external zero-delay PLL and avoid completely the use of DCMs. Nonetheless, the possibility to use DCMs to generate BC x 16 clock from the externally multiplied BC clock or from the 53 MHz SCL clock should be kept.

9/ Delay values, parameter programmation and loading

For each SCLD port, independant delay values can be set for:

- the BC clock sent to the ADF
- the signals going downstream: CMDD, SPARE
- the signals going upstream: CMDU, BUSY_B, ERR_B, STRIG_B

Each delay value is a 5 bit number in units of 1:32th of the BC period (i.e. 4.125 ns in normal operation and 5 ns in standalone tests). The 3 delay values form a 15 bit word which is prefixed with one bit for convinience (i.e. the application parameter is a 16 bit-word per channel). The 5 port SCLD will use 80 bits of configuration data (stored in a 4 Mbit PROM - but can one find small devices nowadays?).

The format of each 16 bit word is:

- bit 15 (MSB) : 0 - unused
- bit 14 downto 10: upstream signals delay
- bit 9 downto 5: downstream signals delay
- bit 4 downto 0: clock delay

A file in MCS format is used to configure the serial PROM over JTAG with Xilinx iMPACT. Note that bytes are serialized LSB first. In the MCS file, keep in mind that the bytes at lower address are placed first. Examples of configuration files for the single port SCLD card are:

delays_u0_d0_c0.mcs
delays_u1_d1_c0.mcs
delays_u2_d2_c0.mcs
delays_u0_d0_c4.mcs

The figure after "u" is the delay for signals going upstream ("d" for signals going downstream, and "c" for the clock signal).

Upon action on the front panel RESET button, the default delay values coded in the firmware are used. When the LOAD button is pressed (or possibly when a Geographic Section initialization request is received), a state machine is triggered to fetch delay values from the external serial PROM.

10/ Overview of the firmware

The top level entity to synthesize and download in the FPGA of the SCLD board is `sc1f_fpga_r` for the reduced version of the SCLD, and `sc1f_fpga` for the full version of the board. These entities are just wrappers that mainly add I/O pads to the `sc1f` entity. The `sc1f` includes all the logic blocks that perform the functions of the card. For each port of the SCLD, an `adfif` block is instantiated. The `adfif` block is the interface to one ADF crate. It includes the logic to serialize the BC clock and the command going downstream to the ADF as

well as the logic to de-serialize the command going upstream. Delay lines are implemented with dsrvl entities which are based on 2 variable length shift registers (clocked on a different edge of the BCx16 clock) followed by a combinatorial multiplexer. The dsrlv entity introduces a digital delay of 1 to 16.5 clock periods in increments of 0.5 clock period.

Other components of the firmware are:

- clk_gen_try: includes the DCMs to make the BCx16 clock. This component may be modified if the BCx16 clock is generated externally or if the 53 MHz clock is used as a reference.
- sprom_loader: state machine to load delay values from the external SPROM
- marker: some logic to generate a synchronization pulse that has a well defined phase w.r.t. the SCL BC clock
- sr_pl_po: a shift register that drives all delay lines configuration pins with either the default delay values or the delays fetched from the external SPROM
- wide_and and wide_or: N inputs AND and OR gates to combine some of the logic signals received from the different connections to the ADF system.

References

[1] B. Haynes et al., "D0 Trigger Distribution System, Serial Command Link Receiver (SCLR)", FNAL, 6 June 2000.

[2] J. Bystricky et al., "Algorithms and Architecture for the L1 Calorimeter Trigger at D0 Run IIb", proceedings of RT2003 conference, Montreal, Canada, 18-23 May 2003.

[3] All the information relevant to the ADF system can be found online at:
http://www-clued0.fnal.gov/~perez/R2BTRIGGER/ADF_Description/ADF_Descri.html

[4] "XC2V1000 Reference Board User's Guide", Memec Insight, July 2001
Kit leaflet available on: <http://www.insight-electronics.com>